LOW-FREQUENCY DISCRETE POWER AMPLIFIERS CIRCUIT DESIGN USING LINEAR AND NONLINEAR TECHNIQUES

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Abstract. This paper presents the structure and operation principles of low-frequency power amplifiers using discrete components. Based on the analysis of a selected circuit configuration, formulas for the critical electrical parameters are derived, and an approach is proposed for determining the total harmonic distortion by studying in the time domain the operational principle. The obtained analytical expressions, as well as some additional conditions, are the basis of the proposed design procedure. The practical efficiency of the proposed methodology has been verified by investigating sample electronic circuits of power amplifiers at various levels of the input sine-wave signals.

Keywords: analog circuits; amplifiers; time-domain analysis; nonlinear distortion; THD; circuit design; circuit simulation.

1. INTRODUCTION

The analysis of scientific and technical literature shows the presence of various circuit configurations of power amplifiers. Moreover, this type of analog circuit is widely used, both for audio amplifiers and for the development of output stages for industrial controllers, powerful oscillators, and power supplies. Depending on the value of the upper 3-dB frequency f_h [5], power amplifiers are divided into low-frequency (with f_h <100 kHz) and high-frequency (with $f_h \geq$100 kHz). In practice, in many cases, low-frequency amplifiers with output power up to about 100 W are used. The implementation of this class of analog circuits is carried out with integrated or discrete elements. Moreover, electronic circuits with discrete elements provide the possibility of implementing electronic devices with arbitrary electrical parameters, which is relatively difficult to implement by using IC power amplifiers. During the last few years, a large number of papers [1-5] have been published, which consider different aspects of analysis and design, and depending on the specific application, different recommendations are defined. There are almost no methodologies that cover

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the entire process of design and analysis in the frequency and time domains of low-frequency power amplifiers. On the one hand, this is partly due to the difficulty of theoretically understanding the problem in such a way as to arrive at useful practical formulas. On the other hand, finding practically useful analytical expressions to estimate the value of the total harmonic distortion (THD) at a given level of nonlinear distortions in the output stage is a challenge. Based on the analyses presented in [5] and [6] of this paper, the authors have attempted to present a procedure for designing low-frequency power amplifiers with discrete elements.

2. ELECTRICAL CIRCUIT AND THEORETICAL ANALYSIS

2.1 Frequency domain analysis. Energy parameters

The object of analysis is the practical circuit of a low-frequency power amplifier [5-7] with a class AB output stage (Fig. 1). It consists of a driver stage and an output stage with a common negative feedback network. A bipolar symmetrical power source is used to produce the external supply voltage of the circuit with $V_{CC} = -V_{EE}$. The driver stage of the amplifier contains a non-inverting AC amplifier with an op-amp, a CC–CB configuration of a cascode amplifier (transistors T_7 and T_8) ($A_{U,cascode} \approx 0.5[g_{m8} \times (g_{m5}^{-1}||R_5)]$), common-base transistor T_5 with a dynamic load, implemented with T_6 ($A_{U5} \approx g_{m5} \times [r_{CE6}(1 + g_{m6}R_6)] >> 1$). The passive components R_N, C_N and R_F of the non-inverting amplifier form the circuit of series–shunt feedback (series connection at the input port and the parallel (or shunt) connection at the output port). In addition, R_P и C_P are included in the input network of the amplifier. Before the driver stage, a first-order low-pass filter is included, consisting of the resistor R_H and the capacitor C_H. This filter determines the f_h of the circuit. For frequencies where $1/\omega C_N << R_N$ and $1/\omega C_P >> R_P$, the closed-loop midband gain is determined by the formula $A_{U0} \approx 1 + R_F/R_N$.

In a wide frequency range, the closed-loop gain is a complex function of frequency ω, and is given by the expression

$$\dot{A}_U = \frac{\dot{U}_o}{\dot{U}_i} = \frac{U_{om}e^{j\phi_o}}{U_{im}e^{j\phi_i}} = \frac{U_{om}}{U_{im}}e^{j(\phi_o-\phi_i)} = \left|\dot{A}_U\right|e^{j\phi} \quad (1)$$

where $\phi = \phi_o - \phi_i$ is the phase difference between the input and output voltages (or phase-frequency response), and $|\dot{A}_U| = |\dot{A}_U(j\omega)|$ is the amplitude-frequency response of the amplifier.

Then, if $C_P R_P = C_N(R_N + R_F)$ is chosen, the lower 3-dB frequency of the amplifier is determined by the formula $f_b = 1/2\pi R_N C_N$. Moreover, in the amplitude-frequency characteristic there will be one real zero at frequency f_b. In the high-frequency range, the amplitude-frequency characteristic is also approximated by two

real poles with frequencies $f_{p1} = 1/2\pi(R_H + R_G)C_H$ and $f_{p2} = f_p(1 + \beta^- A_{d0})$, where $\beta^- = R_N/(R_F + R_N)$ is the transfer function of the feedback network (or *feedback factor*), A_{d0} is the open-loop DC voltage gain, and f_p is the dominant pole frequency of the op-amp. In the design process, from a constructive and circuit engineering point of view, it is recommended to choose $f_{p1} < f_{p2}$. In this way, the selection of passive components forming the general negative feedback is simplified.

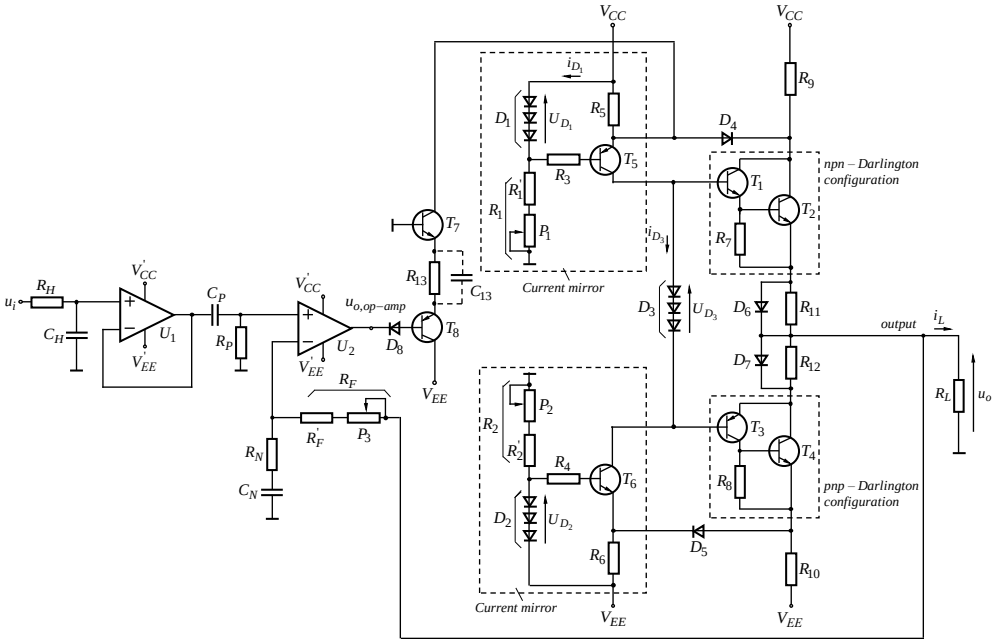


Fig. 1. Circuit configuration of low-power amplifier with discrete components [5-7].

The bandwidth of the amplifier (or 3-dB bandwidth) can be found as the difference between the lower and upper or higher 3-dB frequencies:

$$BW = f_h - f_b \tag{2}$$

For low-frequency power amplifiers, since $f_h >> f_b$, formula (2) is simplified and yields the form $BW \cong f_h$.

Then, the *figure of merit* parameter (or gain–bandwidth product) of the amplifier is obtained

$$GBWP = |A_{U0}|BW \tag{3}$$

The class AB output stage of the amplifier includes transistors $T_1 - T_2$ – forming an *npn* Darlington pair and $T_3 - T_4$ – a *pnp* Sziklai pair. The circuit operates in a

push–pull manner, as $T_1 - T_2$ sources (or pushes) current into the load R_L when $u_i > 0$, and the $T_3 - T_4$ sinks (or pulls) current from the load when $u_i < 0$. The bias voltage of the output transistors in the quiescent mode is obtained and set by means of the three diodes, designated D_3. The current through the diodes is formed by the two current mirrors. To adjust the operating point, resistors $R_1 - R_2$ are replaced with multi-turn potentiometers.

The output current is limited by the diodes $D_4 - D_5$ and resistors $R_9 - R_{10}$. When the voltage U_{R_9} or $U_{R_{10}}$ increases up to 1.8*V*, diode D_4 or D_5 is turned on and the collector current of T_5 or T_6 is reduced. As a result, the base currents of the output transistors are reduced, and hence the load current is also limited.

In the dynamic mode of operation, when connecting an external load R_L, the power-conversion efficiency of the output stage can be found by

$$\eta \equiv \frac{Loadpower(P_L)}{Supplypower(P_{CC})} \times 100\% \tag{4}$$

The difference between the load power and the supply power $P_{CC} = I_{CC} \times V_{CC}$ determines the power dissipation. The maximum power dissipation for each of the output transistors $T_2 - T_4$ can be determined by the formula

$$P_{C\,max\,2(4)} = V_{CC}^2/(\pi^2 R_L) + P_{DQ} \tag{5}$$

where the maximum value is obtained at $U_{Lm} = 2V_{CC}/\pi$ and $P_{DQ} = I_{CQ2(4)}V_{CC}$ is the quiescent power dissipation of each output transistor.

Then, for the second pair of transistors T_2 and T_4, the maximum power dissipation is found by $P_{C\,max\,1} \approx P_{C\,max\,3} > (P_{C2max}/\beta_2) + P_{DQ1}$, where $P_{DQ1} \approx V_{CC}I_{CQ1} \approx$ $\approx V_{CC}\left(I_{CQ2}/\beta_2 + I_{R_7}\right)$, and β_2 is the current gain of T_2. For $u_o = 0$ the required voltage value on the three diodes U_{D3} will be

$$U_{D3} = u_{BEN} + u_{BEP} = 3\phi_T\, ln[\, I_{BIAS} - (I_{CQ2}/\beta_1\beta_2)]/I_S \tag{6}$$

where $I_{BIAS} = \left|I_{CQ5}\right| \approx I_{CQ6} > I_{B1max} + I_{D_3}$, as $I_{B1max} = I_{Lm}/\beta_2\beta_1$ and $I_S = 10^{-13}A$ is the saturation current.

The quiescent current for transistors T_2 and T_4 is determined by the formula $I_{CQ2(4)} = nI_{BIAS}$, where the coefficient n = 3÷10 is defined as a ratio of the emitter–junction area of the output devices to the junction area of the biasing diodes [5].

2.2 Time domain analysis - total harmonic distortion

An important parameter of the output stages in power amplifiers is to have a low output impedance, since in most cases the external loads have a small ohmic resistance. In this case, the output signal can be applied to the load without loss of

amplification. Also, often the output signals have a large amplitude, so in the process of analysis and design, approximate models for small signals are either not applicable or must be used very carefully, taking into account the entry into the nonlinear regions of operation. In fact, a measure of the efficiency of the output stages is the evaluation of the THD. It is defined as the ratio of the RMS value of the amplitudes of the higher harmonics (2^{nd}, 3^{rd},…) of the output signal to the amplitude of the fundamental harmonic $I_{emax,1} \cong I_{Lm}$, expressed as a percentage [7]. To determine and estimate the THD coefficient, an approach is proposed that analyzes the nonlinearities in the characteristics of bipolar transistors when a sinusoidal signal with a relatively large amplitude is applied to the output stage of the amplifier. A similar method is used in the analysis of the self-oscillation conditions of oscillatory circuits [8,9].

When a voltage is applied between the base and the emitter of a bipolar transistor

$$u_{BE}(t) = U_{BEQ} + U_{be,max}\cos\omega t \tag{7}$$

the collector current is obtained as a periodic series of pulses whose amplitudes depend on the nonlinear nature of the volt-ampere characteristic, approximated by the following analytical formula

$$i_E(t) = I_S e^{\frac{u_{BE}(t)}{\phi_T}} = I_S e^{\frac{U_{BEQ}}{\phi_T}} e^{x\cos\omega t} \tag{8}$$

where $\phi_T = kT/q \approx 26mV$ – thermal voltage at 300K and $x = UT_{bemax}/\phi_T$ is the parameter of the drive level.

If the expression $e^{x\cos\omega t}$ is presented in a Fourier series, it is found

$$i_E(t) = I_S e^{\frac{U_{BEQ}}{\phi_T}}[\alpha_0(x) + 2\sum_{n=1}^{\infty}\alpha_n(x)\cos(n\omega t)] = I_{e,DC} + \sum_{n=1}^{\infty}\underbrace{2I_{e,DC}\frac{\alpha_n(x)}{\alpha_0(x)}}_{I_{emax,n}}\cos(n\omega t) \tag{9}$$

where $I_{e,DC} = I_S e^{U_{BEQ}/\phi_T}\alpha_0(x)$ is the DC value of the emitter current, and $I_{emax,n}$ is the amplitude of the n^{th} harmonic (n = 1, 2, …).

The coefficients α_0 and α_n in the Fourier series can be determined by the following analytical expressions

$$\begin{aligned}\alpha_0(x)|_{n=0} &= \frac{1}{2\pi}\int_0^{2\pi} e^{x\cos\omega t}\,d\,\omega t \text{ and}\\ \alpha_n(x)|_{n>0} &= \frac{1}{2\pi}\int_0^{2\pi} e^{x\cos\omega t}\cos n\,\omega t d\,\omega t\end{aligned} \tag{10}$$

The determination of the numerical values of the α_0 and α_n can be carried out by expanding the integral functions in a Maclaurin series [10], in which case we obtain the following Bessel functions with integrated Gamma function:

$$\alpha_n(x) = \sum_{k=0}^{\infty} \frac{(-1)^k}{k! \times \Gamma(k+n+1)} \times \left(\frac{x}{2}\right)^{2k+n} \tag{11}$$

Then, for the total harmonic distortion, it is obtained

$$THD = \frac{\sqrt{I_{e\,max,2}^2 + I_{e\,max,3}^2 + \dots}}{I_{e\,max,1}} \times 100\% \tag{12}$$

In the process of designing the electronic circuit, initially from the datasheet of the chosen output transistors, the voltage $U_{be,max}$ for the maximum output current I_{Lm} is determined. Then, the value of the parameter x is calculated. For the values thus obtained, the $I_{e,DC} = I_{Lm}/[2\alpha_1(x)/\alpha_0(x)]$ value of the emitter current is determined. Finally, the amplitudes of the higher harmonics are sequentially calculated, as follows $I_{e\,max,2} = 2I_{e,DC}[\alpha_2(x)/\alpha_1(x)]$, $I_{e\,max,3} = 2I_{e,DC}[\alpha_3(x)/\alpha_2(x)] \dots$.

3. DESIGN PROCEDURE

Based on the theoretical analysis presented above, performed in the frequency and time domains, a design procedure for the circuit in Fig. 1 is proposed in this section. Moreover, this methodology, with some modifications, can be used as a basis for designing other circuit configurations of low-frequency power amplifiers. The proposed procedure combines manual calculations of the parameters for passive components with computer simulations, so as to reach a working prototype of the electronic circuit in a shorter time. More specifically, the design of the electronic circuit is carried out in the following sequence:

Step 1: *Technical requirements*. The following parameters are specified: input voltage amplitude U_{im} or source voltage e_G and internal resistance R_G; input resistance r_{iA}; output power P_{Lmax} (sinus) and external load resistance R_L; maximum ambient temperature T_a; output resistance r_{oA}; low cut-off frequency f_b and M_b [dB]; high cut-off frequency f_h and M_h [dB]; *THD* [% or *dB*] ; output offset voltage $U_{o,err}$;

Step 2: *Determining the voltage amplitude on the load*. $U_{Lm} = \sqrt{2P_L R_L}$;

Step 3: *Calculating the amplitude of the current through the load*.

$I_{Lm} = \sqrt{2P_{Lmax}/R_L}$;

Step 4: *The supply voltage $V_{CC} = -V_{EE}$ of the final stage is determined*: $V_{CC} \geq U_{Lm} + U_{CER} + U_{aux}$, where U_{CER} is the minimum voltage between the collector and emitter of the transistors T_1 and T_2 (or T_3 and T_4), for which they operate in normal

mode of operation and $U_{aux} = U_{CE5(6)} + U_{R5(6)} + U_{ocm}$, where the voltages $U_{CE5} = U_{CE6} \approx 1...2V$, $U_{R5} = U_{R6} \approx 1V$ and ballast (residual) voltage U_{ocm} (between no-load mode of operation and full load of the output) with values not greater than ($0.1-0.2$) U_{Lm}.

Step 5: Selecting the quiescent current of the output transistors. $I_{CQ2} \approx I_{CQ4}$ for the class of operation AB. The quiescent current is usually much smaller than the I_{Lm}(<10%). $P_{DQ} = I_{CQ2(4)}V_{CC}$;

Step 6: The maximum power dissipation of the output transistors is calculated: $P_{Cmax} = (V_{CC}^2/\pi^2 R_L) + P_{DQ2(4)}$, where the power is obtained for $U_{Lm} = 2V_{CC}/\pi$.

Step 7: Selecting the output transistors T_2 and T_4, which should have $I_{Cmax} \geq I_{Lm}$, $U_{CEmax} \geq V_{CC} + U_{Lm}$, $P_{tot} \geq P_{Cmax}$, and the current amplification factor β with a large value if possible.

Step 8: Calculation of the thermal resistance $R_{th\,r-a}$ and area of the heat-sink: $R_{th\,r-a} \leq [(T_c - T_a)]/P_{tot} - R_{th\,c-r}$ [°C/W], where for the selected transistor, the case temperature T_c is determined based on the power P_{tot}, and the thermal resistance $R_{th\,c-r}$ is determined by the type of material, for example, for thermal contact, silicone paste$R_{th\,c-r} \leq 0{,}8°C/W$. The surface area S_{HS}, representing an aluminum plate with a thickness of about $3mm$, is calculated by the formula $S_{HS} = 1/\alpha_{th}R_{thr-a}$, where $\alpha_{th} \approx 1 \div 2[mW/cm^2°C]$ [6].

Step 9: Calculation of resistances R_9 and R_{10}. D_4 and D_5 are selected: The limit value of the output current $I_L \leq I_{Lm}$; $R_9 = R_{10} = 1.8V/I_{Lm}$; $P_R = 0.5(1.8V \times I_{Lm})$ – for each half-wave of the output current. In the output current limiting mode of operation, a differential current of several mA flows through the diodes D_4 and D_5 . Usually, D_4 and D_5 are implemented with low-power diodes.

Step 10: The resistances R_{11} and R_{12} are calculated. The diodes D_6 and D_7 are selected:

– The resistances R_{11} and R_{12}, forming the negative feedback, are calculated: At $u_i = 0$, the voltage drops $U_{R11} = U_{R12} \approx 0.1...0.2V$ are selected. In this case, the diodes D_6 and D_7 they are turned off, and no current flows through them.

For the resistances R_{11} and R_{12}, is obtained: $R_{11} = R_{12} = U_{R11}/I_{CQ2}$;

– The diodes D_6 and D_7 are selected. In the dynamic mode of operation, the diodes D_6 and D_7 will conduct one half-wave of the output current, with the maximum value of the current being I_{Lm}: $I_{Dmax} > I_{Lm} \rightarrow$.

Step 11: The resistances R_7 and R_8 are calculated: $R_7 = U_{BE2}/I_{R_7}$, as $R_7 = R_8$ and $U_{BE2} \approx U_{BE4} \approx 0{,}6V$.

Step 12: Transistors T_1 and T_3 are selected, according to the conditions: $I_{CQ1} \approx I_{CQ3} \approx I_{BQ2} + I_{R_7}$, where $I_{BQ2} = I_{CQ2}/\beta_2$; $U_{CE1max} \approx U_{CE3max} \approx U_{CE2max}$; $I_{C1max} \approx I_{C3max} \approx I_{B2max} + I_{R_7}$, where $I_{B2max} = I_{Lm}/\beta_2$;

Step 13: For the current mirrors are obtained: $|I_{CQ5}| \approx I_{CQ6} > I_{B1max} + I_{D_3}$, where $I_{B1max} = I_{Lm}/\beta_2\beta_1$; $R_{5(6)} \approx (U_{D1(2)} - U_{BE5(6)})/I_{EQ5(6)}$, where $U_{D1} \approx U_{D2} \approx 3 \times 0{,}6V = 1{,}8V$; $R_1 = R_2 \approx (V_{CC} - U_{D1})/I_{D1}$. In addition, the potentiometers P_1 and P_2 can be used for the adjustment of the operating point of the output stage.

The resistances R_3 and $R_4$are chosen to be equal to a few *k*Ω. They limit the base currents of T_5 and T_6 in the short-circuit mode at the output of the amplifier.

Step 14: *The transistors* T_7 and T_8 *are selected*. They are low-power BJTs with a sufficiently high transition frequency (for example, at least ten times higher than the frequency f_h). They are selected mainly based on the voltages between *C–E*, which are determined by the expression $U_{CE7max} \approx U_{CE8max} \approx U_{CE2max}$;

Step 15: *The total harmonic distortion THD' is determined*. Nonlinear distortions are caused mainly by the output stage ($T_2 - T_4$ and $T_1 - T_3$): $THD' \approx THD_{2,4} + THD_{1,2}$ at a midband frequency $f_b < f_M < f_h$;

Step 16: *The required depth of the total negative feedback is determined*: $F = m(THD'/THD)$, where the parameter m for large values of the U_{Lm} is chosen in the range from 1.5 to 2. In addition, the P_3 potentiometer can be used to adjust the F;

Step 17: The input voltage amplitude for the resulting feedback depth is determined: $U_{im,req} = U_{om}/A'_{U0}$, where $A'_{U0} = (|A_d(f_M)| \times A_{U,cascode} \times A_{U5})/F$;

Step 18: The passive components in the negative feedback loop are selected: $R_N = R_F/(A'_{U0} - 1)$; $R_P = R_F + R_N$; $C_N = C_P \geq (2\pi f_b R_N \sqrt{M^2_{C_{N(P)}} - 1})^{-1}$. Moreover, for the non-inverting amplifier is obtained: $C_P R_P = C_N(R_N + R_F)$.

Step 19: *The op-amps* U_1 and U_2 *are selected, according to the conditions:* $f'_{pA_{U0},OY} > f'_h$, where $f'_h = f_h/\sqrt{M_h^2 - 1}$ and $f'_{pA_{U0},OY}$ is the high cut-off frequency obtained as the intersection point of the straight line $A_{U0} = U_{Lm}/U_{im}$ and the frequency response of the open-loop gain of the op-amp; $SR_{OA} > 2\pi f'_h U_{Lm}$ [*V/s*];

Step 20: *The error voltage is calculated:* $U_{o,err} = U_{io} - R_P I_B^+ + R_F I_B^-$ at $T_{nom} \approx 25°C$.

4. DESIGN EXAMPLE

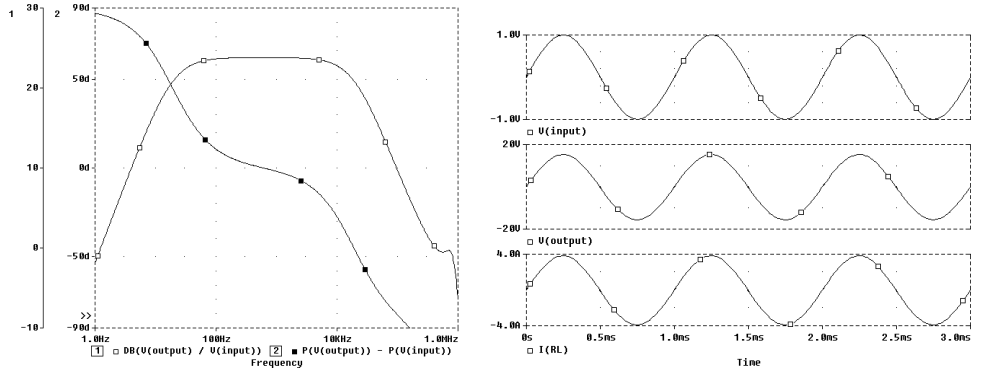
The object of the design process is a low-frequency power amplifier intended to transmit to a certain load $R_L = 4\Omega$ electrical power $P_{Lmax} = 30W$ (sinus) at maximum nonlinear distortions of the amplified signal with a value of $THD \leq 0.5\%$ and an offset of the output voltage not greater than $\pm 20mV$. The operating frequency range is from $f_b = 20Hz$ to $f_h = 20kHz$, with a coefficient of linear distortions not greater than 3*dB*. The maximum ambient temperature is up to 45°C. The parameters of the input circuit are: input voltage with amplitude $U_{im} = 1V$, input resistance

$r_{iA} \geq 10k\Omega$ and internal resistance $R_G = 50\Omega$ of the source e_G. Moreover, in this case, the input signal source can be an electronic module for reproducing sound from a personal computer with a typical value of the output signal level up to about $1V$, and the load can be a loudspeaker or speaker with an internal ohmic resistance 4Ω and maximum sound power up to about $40W$. A suitable value of the supply voltage can be determined based on the output power and the load, namely $U_{Lm} = \sqrt{2P_L R_L} = 15.49V$. Depending on the selected electronic circuit, the supply voltage $V_{CC} = -V_{EE}$ should be from 10 to 30% greater than U_{Lm} or from 18 V to $21V$, and in some cases a greater value (for the example $25V$ is chosen). The average power extracted from each of the two supplies $P_{CC}^{+} = P_{EE}^{-} = U_{om}V_{CC}/\pi R_L \approx 22\ldots26W$, then for the full power consumed by the power source $P_{CC} \approx 44\ldots52W$. Based on the proposed procedure in Section 3, Table 1 presents the values of the passive components and the type of the selected active elements.

Figure 2 shows the simulation characteristics of the designed amplifier in the frequency and time domains at maximum output current. As can be seen, the *GBWP* is achieved, and the nonlinear distortion coefficient is below 0.5%.

Table 1. Active and passive components

Component	**Value**
Input low-pass filter (R_H and C_H)	10kΩ and 820pF
C_P and C_N	10μF
Feedback resistors (R_F and R_N)	12kΩ (120kΩ) and 690Ω
Op-amps (U_1 and U_2)	TL082CDR
NPN transistors (T_6 and T_7)	BC546A
PNP transistors (T_5 and T_8)	BC556A
R_{13} and C_{13}	1kΩ and 1nF
Diodes (D_4 …D_8, D_{11}, D_{12}, D_{13}, D_{21}, D_{22}, D_{23}, D_{31}, D_{32} and D_{33})	1N4148
R_1 and R_2	3.9kΩ
R_3 and R_4	1.5kΩ
R_5 and R_6	120Ω and 240Ω
R_7 and R_8	300Ω
R_9 and R_{10}	0.5Ω
NPN transistor T_1	BD135 [11]
PNP transistor T_3	BD136
Diodes (D_6 and D_7)	6A10
NPN output transistors (T_2 and T_4)	TIP41C [12]
R_{11} and R_{12}	7.5Ω



a) b)

Fig. 2. The simulated responses at $I_{Lm} \approx 3.87A$: a) AC transfer characteristics; b) input and output signals (**V(input)**, **V(output)**, **I(RL)**, and **THD=0.22%**).

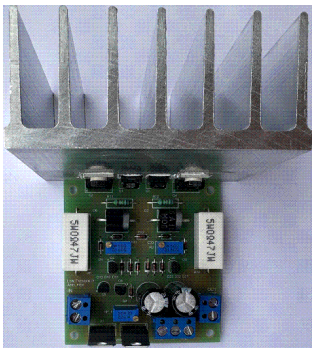


Fig. 3. Top view of the PCB for the test circuit configuration of Fig. 1.

In addition, Table 2 presents simulation and experimental results at different output voltage (or output power) values, and the study was performed for two frequencies, $1kHz$ and $10kHz$. To calculate the THD, the parameters of the transistors in the output stage BD135 [11] and TIP41C [12] were used. Also, the parameters of the selected op-amp TL082CDR were also used to determine $U_{im,req}$. and A_{U0}. Based on an analysis of the frequency response, $|A_d(1kHz)| \approx 72dB$ and $|A_d(10kHz)| \approx \approx 52dB$ were determined. As can be seen in Table 2, when U_{om} is reduced, the THD decreases, and at $< 5V$, the value is below 0.1%. For $U_{om} > 5V$, the THD increases to about 0.6%, which confirms the theoretical hypotheses presented in sections 2 and 3. For a frequency of $10kHz$, the THD has a higher value, since $|A_d|$ is smaller. The experimental results were obtained using a sample electronic circuit implemented on a PCB with a combination of through-hole and surface mount components (Fig. 3). The surface mount components are located on the bottom side of the printed circuit board.

Table 2. Simulation and experimental results

Parameter	f_M = 1kHz, R_N=690Ω, and R_L = 4Ω					f_M = 10kHz, R_N=690Ω, and R_L = 4Ω				
	1	***2***	***3***	***4***	***5***	***1***	***2***	***3***	***4***	***5***
$U_{om,spec}, V$	2.5	5	10	12	15	2.5	5	10	12	15
I_{Lm}, A	0.625	1.25	2.5	3	3.75	0.625	1.25	2.5	3	3.75
$U_{be,max}, V$	0.64	0.65	0.66	0.68	0.7	0.64	0.65	0.66	0.68	0.7
x	24.6	25	25.4	26.2	27	24.6	25	25.4	26.2	27
$R_F, k\Omega$	127.3	126.8	125	62.55	62.3	12	12	12	12	12
$U_{i,req}, mV$	15	30	54	130	165	135	270	540	650	820
THD, %	≤ 0.5	≤ 0.5	≤ 0.5	≤ 0.5	≤ 0.5	≤ 0.5	≤ 0.5	≤ 0.5	≤ 0.5	≤ 0.5
THD_{sim}, %	< 0.1	< 0.1	0.1	0.155	0.22	< 0.1	< 0.1	0.19	0.24	0.45
THD_{meas}, %	0.055	0.088	0.12	0.17	0.19	0.05	0.086	0.14	0.23	0.59
I_{CC}, A	0.238	0.430	0.835	0.992	1.28	0.214	0.436	0.862	0.980	1.24

5. CONCLUSION

In this article, a solution to several problems in analog circuitry is presented:

(1) A theoretical analysis is presented, clarifying the processes developing in low-frequency power amplifiers at a frequency and time domain of operation.

(2) Based on the time-domain analysis, an approach for theoretical determination of the total harmonic distortion based on the study of the nonlinear volt-ampere characteristics of bipolar transistors and their analytical expressions for approximation is proposed.

(3) As a result of the analyses and basic theoretical predictions for selected circuit configurations with discrete components, a design methodology is proposed;

(4) An approach is proposed for selecting the passive components and the operating points of the output transistors within the feedback network at a given level of the output signal's amplitude to obtain a small value of the total harmonic distortion and the desired value of the gain–bandwidth product.

All of the above-presented conclusions allow designers to improve the efficiency of the developed analog circuits and to significantly reduce the process of experimental work on the developed prototypes.

REFERENCES

[1] M. AHMED, A. DALBAH, O. HAMMI AND ET. AL., Behavioral Modeling and Predistortion of Dual-Band Power Amplifiers (2025) *IEEE Access*, **13**, 129305-129330, online: DOI: 10.1109/ACCESS.2025.3590752.

[2] N. KOO, Design of Low Power and Low Noise Instrumentation Amplifier for Biopotential Acquisition: A Review (2025) *IEEE Access*, **13**, 23359-23370, online: DOI: 10.1109/ACCESS.2025.3537998.

[3] B. LIU, L. XUE, H. FAN AND ET. AL., An Efficient and General Automated Power Amplifier Design Method Based on Surrogate Model Assisted Hybrid Optimization Technique (2025) *IEEE Transactions on Microwave Theory and Techniques*, **73** (2), 926-937, online: DOI: 10.1109/TMTT.2024.3518913.

[4] E. AGGRAWAL AND K. RAWAT, Exploring Feasible Design Space for Multi-Octave Power Amplifier Using Nonlinear Embedding (2021) *IEEE Transactions on Circuits and Systems II: Express Briefs*, **68** (8) 2800-2804, online: DOI: 10.1109/TCSII.2021.3069867.

[5] A. SEDRA, K. SMITH, T. CARUSONE AND V. GAUDET, *Microelectronic circuits*, (8th edition), Oxford, New York Oxford University Press (2020), ISBN 978-0-19-933913-6.

[6] M. SEIFART, *Analoge Schaltungen* (6 Auflage), Verlang Technik Berlin, Germany, (2003), ISBN 978-3341012987.

[7] V. TIETZE AND C. SCHENK, *Electronic circuits* (2nd edition), Springer New York, NY, USA, (2008), ISBN 978-3-540-00429-5.

[8] U. ROHDE AND A. APTE, Everything You Always Wanted to Know About Colpitts Oscillators (2016) *IEEE Microwave Magazine*, **17** (8), 59-76, online: DOI: 10.1109/MMM.2016.2561498.

[9] U. ROHDE, A. PODDAR AND G. BÖCK, The Design of Modern Microwave Oscillators for Wireless Applications. Wiley, New York, USA (2005), ISBN 9780471723424.

[10] M. ABELL AND J. BRASELTON, *Introductory Differential Equations* (4th Edition). Academic Press, New York, USA (2014), ISBN 978-0124172197.

[11] BD135: 1.5A Power Transistors – datasheet. Onsemi, online: https://www.onsemi.com

[12] TIP41C: NPN Silicon Power Transistors – datasheet. M.C.C., online: https://www.mccsemi.com

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