A STUDY OF THE INFLUENCE OF CIRCUIT COMPONENTS ON THE DYNAMIC BEHAVIOUR OF A ZVS PHASE-SHIFT CONTROLLED DC-DC CONVERTER WITH SYNCHRONOUS RECTIFIER

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Abstract. The paper studies the influence of the added commutating inductance, ensuring ZVS conditions, on the dynamic behavior of the zero-voltage (ZVS) phase-shift controlled full-bridge (PSFB) converter. The mutual influence of the converter parasitic elements on the circuit's operation is also investigated. This analysis considers different distinct values of the commutating inductance, providing a comprehensive perspective on the system's behavior under varying conditions. The theoretical study of the ZVS-PSFB converter's open-loop main transfer characteristics is verified through simulations. The theoretical results are verified through the LTspice simulation study of the converter's operation during the abrupt load changes.

Keywords: phase-shift controlled DC-DC, transfer functions; ZVS

1. INTRODUCTION

The phase-shifted full-bridge (PSFB) converter is a popular topology for medium- to high-power DC-DC conversion due to its fixed-frequency operation and ability to achieve zero-voltage switching (ZVS) across all primary and secondary switches. It offers high efficiency, low output ripple, and a wide output voltage range, making it particularly effective under light- and full-load conditions [1, 2]. However, the topology presents several challenges, including complex conversion ratio calculations, ZVS limitations at light loads, higher RMS currents in the primary switches, etc. Despite these drawbacks, the PSFB converter remains a solution where efficiency, voltage flexibility, and parallel operation are critical [3, 4]. The PSFB converter also provides a robust solution for network and telecommunications equipment, providing isolated low-voltage outputs (from a 48 V input bus) [5, 6]. Additional requirements include high efficiency to reduce heat dissipation and low component height. Meeting these requirements becomes more difficult with increased power levels due to the

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corresponding power dissipation of components and increased transformer size. Simple power supply topologies are being replaced by more complex, single- and two-stage approaches that utilize transformers and semiconductors.

In [7], a phase-shift-controlled ZVS full-bridge DC-DC converter utilizing synchronous rectification with an LTC3722 controller was investigated. An analysis was performed to examine the effect of the added commutating inductance on the ZVS characteristics under varying load conditions. In the present paper, the research is expanded by analyzing the influence of the added commutating inductance on the dynamic performance of the ZVS-PSFB converter, as well as the combined effect of this inductance with converter parasitic elements on the circuit's operation. Design considerations of a type 2 compensator with an optocoupler are also included. A simulation study with LTspice of the converter's operation under the abrupt load changes is presented.

2. MAIN CIRCUIT OPERATION

2.1 Operation principle and main dependencies

Figure 1 illustrates the circuit diagram for the converter being studied, which includes loss resistors. The converter consists of transistors $Q1 \div Q4$ and their body diodes $D1 \div D4$, an added commutating inductance L_k, a center-tapped transformer (Tr), and a synchronous rectifier (transistors QE, QF). R_{ESR} denotes the equivalent series resistance of the output capacitance C_0. R_{loss} presents the converter's losses and resistance. The MOSFETs' output capacitances, *C1oss÷ C4oss*, are also included (shown with dashed lines). Resistance R_0 is the circuit load. The "passive" leg includes transistors $Q1$ and $Q2$; the "active" leg includes transistors $Q3$ and $Q4$.

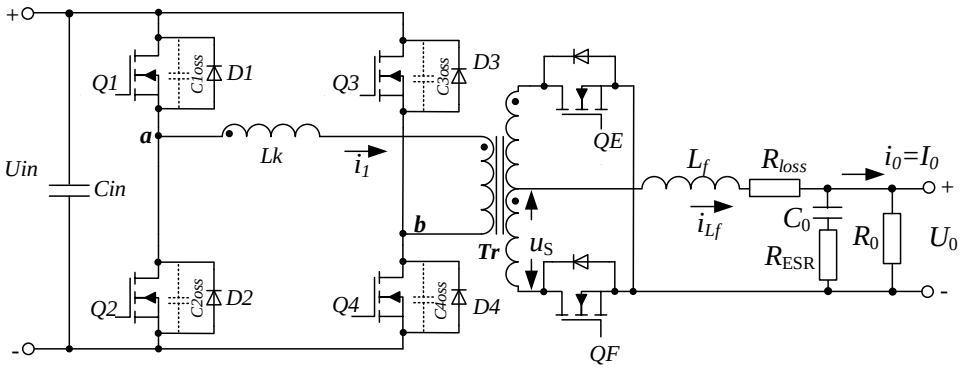

Fig. 1. Full-bridge phase-shift controlled ZVS DC-DC converter with a center-tapped synchronous rectifier.

Figure 2 shows the waveforms that describe the principle of operation.

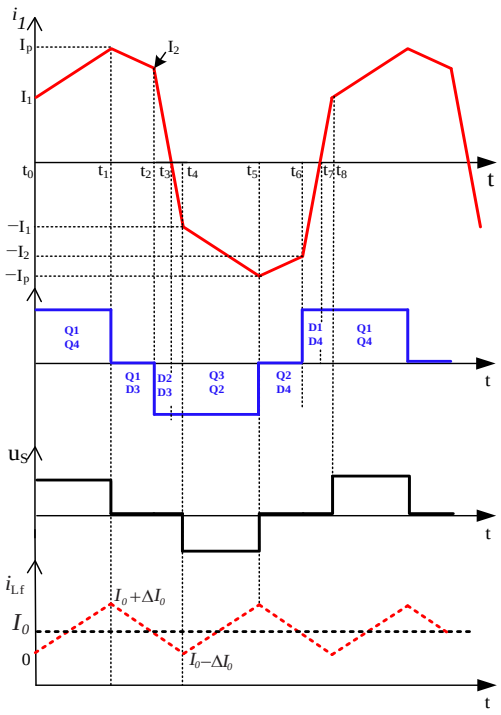

Fig. 2. ZVS-PSFB waveforms

The converter's operation can be summarized as follows, with different modes of switching and energy transfer: Interval 1: The process begins with the turn-on of transistors $Q1, Q4$, and QF. Transistors $Q2, Q3$, and QE remain off. The input voltage is applied to the primary winding of the transformer, causing the current to rise. At the end of the interval, $Q4$ turns off and QE turns on.

In interval 2, after $Q4$ turns off, the voltage at the node b rises to U_{in}. The magnetizing and output currents aid this process applied to the primary side. At the same time, the rate of increase is limited by the output capacitances $Coss3$ and $Coss4$, and the transformer inter-winding capacitance C_{TR}. If there is sufficient energy in the inductors (added commutating inductance, including primary leakage inductance), $Q3$ turns on at zero voltage (ZVS). Current continues to flow through the primary winding of the transformer via $Q1$ and $D3$, short-circuiting the secondary winding through conducting transistors QE and QF. At the end of this interval, transistors $Q1$ and QF are turned off.

Interval 3: At the end of the half-cycle, the transistor $Q1$ turns off, causing the voltage at node a to drop to zero. The leakage inductance of the primary winding of

the transformer, combined with the added commutating inductance, ensures a smooth transition by transferring energy resonantly to the capacitive elements. When transistor $Q2$ turns on at zero voltage, the current in the primary winding changes direction gradually. Once the current reaches the value of the output current converted to the primary side, the secondary winding begins supplying energy to the load again. The time it takes for the current to change direction limits the duty cycle and requires the addition of a small switching inductance to reliably achieve zero-voltage switching (ZVS) in the passive leg over a wide range of load changes. Interval 4: The primary current continues to increase, but in the opposite direction from Interval 1. This interval consists of the magnetizing current and the output current converted to the primary side. At the end of the interval, transistor $Q3$ switches off, performing an active transition similar to interval 2, but in the opposite direction.

To ensure ZVS switching conditions in the circuit, the leakage inductance of the transformer windings can be utilized. The inductance current must be sufficient to recharge the parasitic capacitances (drain-to-source capacitances) of the MOSFETs so that the voltage across them drops to zero before switching. To ensure reliable ZVS in the passive leg over a wide range of load variations, additional commutating inductance is often necessary on the primary side of the converter. This additional inductance serves as an energy storage tank that provides the necessary recharging of the passive leg capacitances to achieve ZVS, even at lower loads. However, if an L_k it is too large, it can cause an increase in the circulating current and RMS losses, and a reduction of the control range.

The previously mentioned algorithm can be implemented using specialized controllers of various manufacturers, such as the UCC28950 and LTC3722-1/LTC3722-2, etc. [5, 6]. In this work, the LTC3722-1 IC is employed [6, 8]. The reliability of this driver is enhanced by its comprehensive set of protection features.

The converter voltage gain M is equal to

$$M = \frac{U_0}{U_{in}} = \frac{n_s}{n_p} D_S \tag{1}$$

where D_S denotes the duty cycle of the secondary-side voltage u_S.

The primary side duty cycle D is given by [1]

$$D = D_S + \Delta D \tag{2}$$

where ΔD represents the decrease in duty cycle resulting from the limited rise and fall times of the primary current waveform ($t_2 \div t_4$ and $t_6 \div t_8$, etc.). The dependencies for their calculations, according to [1], are given in Table 1.

Achieving ZVS across a wide range of load conditions requires an increase in the commutating inductance L_k (including primary leakage inductance). However, raising the value of L_k reduces the rate of change of the primary current during its rising and falling intervals. This limits the duty cycle that can be attained on the secondary

side. For this reason, the value of L_k must be selected considering both the switching frequency and the transformer turns ratio, so that the maximum duty cycle D_{max} satisfies (5).

Table 1. Choice of the Duty cycle

$$\Delta D = \frac{(n_s/n_p)}{\frac{U_{in}}{2f_s L_k}}\left(2I_0 - \frac{U_0}{2f_s L_f}(1-D)\right)$$	(3)
$$D = D_S\left(1 + 4\frac{L_k . f_s}{R_0(n_p/n_s)^2}\right)$$	(4)
$$1 \geq D_{max} \geq \frac{n_p}{n_s} M\left(1 + 4\frac{L_k . f_s}{R_0(n_p/n_s)^2}\right)$$	(5)

Transistors $Q1$ and $Q2$ achieve zero-voltage switching only when the load current exceeds a specific critical level. The required critical current in the primary side for ZVS can be derived from [1]:

$$I_{crit} = \sqrt{\frac{2}{L_k}\left(\frac{4}{3}C_{oss}U_{in}^2 + \frac{1}{2}C_{tr}U_{in}^2\right)} \quad (6)$$

In the ZVS-PSFB, transformer design does not require minimizing leakage inductance, unlike in standard PWM converters. The main limitation arises from winding parasitic capacitance, which must discharge concurrently with the charging/discharging of MOSFETs' output capacitances. This raises the energy that must be stored in the leakage inductance for ZVS, thereby increasing the critical current requirement. To mitigate this, winding parasitic capacitance should be minimized during transformer design.

2.2 A study of the influence of converter elements on the open-loop control-to-output voltage transfer function

To analyze the dynamic behavior of the converter, it is necessary first to analyze the open-loop transfer characteristics. A comprehensive examination of the combined effect of parasitic elements, the value of the switching inductance that ensures ZVS conditions, and power losses on the converter's operation is essential.

The open-loop control-to-output transfer function, neglecting the equivalent series resistance R_{ESR} of the output filter capacitor and the losses resistance R_{loss} of the converter according to [9] can be evaluated as follows:

$$G_{vd}(s) = \frac{U_{in}(n_s/n_p)}{s^2 C_0 L_f + s\left(\frac{L_f}{R_0} + 4(n_s/n_p)^2 L_k . f_s C_0\right) + \frac{4(n_s/n_p)^2 L_k . f_s}{R_0} + 1} \quad (7)$$

It is evident from (6) that the control-to-output transfer function, $G_{vd}(s)$, presents the behavior of a second-order system. The ZVS-PSFB converter functions similarly to a buck converter, yet, as illustrated by (7) on the open-loop control-to-output transfer characteristic, several factors contribute to its performance. These include the values of the output filter capacitor C_0 and inductance L_f, the transformer ratio, the value of the switching inductance, the switching frequency, and the load.

The dependence of the control-to-output transfer characteristic, $G_{vd\_re}(f)$, taking into account the active resistance of the filter capacitor R_{ESR} and the loss of resistance R_{loss}, is as follows [9]:

$$G_{vd\_re}(f) = \frac{U_{in}(n_s/n_p)(j2\pi f R_{ESR} C_0 + 1)}{(j2\pi f)^2 b_2 + j2\pi f b_1 + b_0} \quad (8)$$

where $b_2 = C_0 L_f \left(1 + \frac{R_{ESR}}{R_0}\right)$; $b_0 = \frac{R_{loss} + 4(n_s/n_p)^2 L_k . f_s}{R_0} + 1$ and

$b_1 = \frac{L_f}{R_0} + R_{ESR} C_0 + \left(R_{loss} + 4(n_s/n_p)^2 L_k . f_s\right)\left(1 + \frac{R_{ESR}}{R_0}\right) C_0$ For R_{loss} is valid

$$P_{loss} = U_0 I_0 \frac{1-\eta}{\eta} = R_{loss} I_0^2 \quad (9)$$

and η is the converter efficiency.

Expressions (7) and (8) demonstrate the necessity of investigating the combined effect of parasitic elements and losses on the dynamic behavior of the full-bridge phase-shift controlled ZVS converter.

For the purposes of the study, a synchronous full-bridge phase-shift controlled ZVS converter was designed with the following parameters: output power P_0 = 120 W; input voltage U_{in} = 48 V(±1V); output voltage U_0 = 12 V±1%; switching frequency f_S = 200 kHz. The commutating inductance L_k= 300 nH. The LTC3722-1 phase-shift PWM controller was chosen, and the MOSFETs used are PSMN013-100YSE with output capacitance C_0 = 265 pF [10]. To meet the output current ripples, an output filter inductance $L_f = 5.3\mu H$ was chosen. To meet the output voltage ripples, an output filter capacitance C_0 =1000μF (R_{ESR}=30mΩ, Panasonic

POSCAP), was chosen. Output inductor L_f peak-to-peak ripple current is set to 20%÷30% of the output current. The ZVS range is chosen to be from full load to 50% load. The transformer interwinding capacitance is supposed to be C_{TR} = 100 pF. Using (6), the initial guess for the critical current in the primary side for ZVS is I_{crit} =2.47 A for U_{in} =48 V.

Figure 3 illustrates the influence of inductance L_k on the control-to-output transfer function G_{vd}, defined by (7), for three distinct values of L_k for 50% load:$L_k = 300nH$ (red line), $L_k = 600nH$ (blue line), and $L_k = 2\mu H$ (green line). The phase plots are given with dashed lines in the same colors.

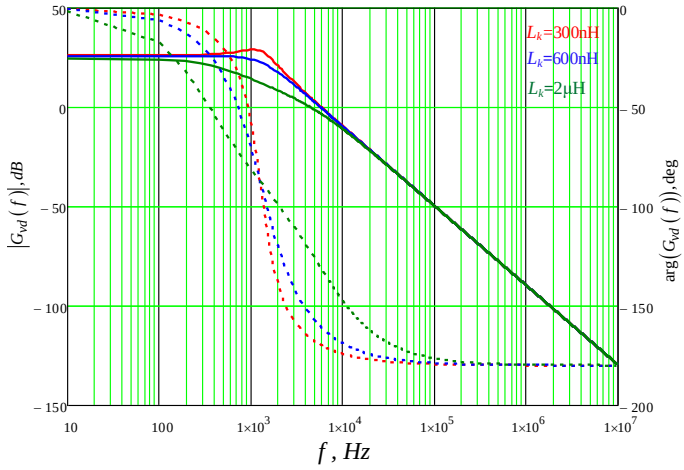

Fig. 3. Theoretically obtained Bode diagrams of the magnitude, dB, and phase plots, deg (dashed lines) of the open-loop control-to-output transfer function, for different L_k values

The results show that increasing the value of L_k reduces DC gain and damps the open-loop control-to-output transfer characteristic.

Figure 4a and Figure 4b graphically show the effect of the commutating inductance on the magnitude and phase of control-to-output transfer functions $G_{vd}(f)$ and $G_{vd\_re}(f)$ defined by (7) and (8) for C_0=1000μF and C_0=100μF, respectively at $R_{loss} = 50m\Omega$. The results presented in Fig. 4a show that DC gain decreases as L_k increases. At the same value of L_k crossover frequency of the ideal PSFB is lower than in the losses PSFB. Furthermore, when L_k increases (L_k=2μH) the open-loop crossover frequency decreases. Consequently, when the commutating inductance L_k increases, the phase margin around the crossover region is reduced. The results presented in Fig. 4b also show that DC gain decreases as L_k increases and damps the open-loop control-to-output transfer characteristics. Furthermore, these characteristics have overlapping crossover frequencies.

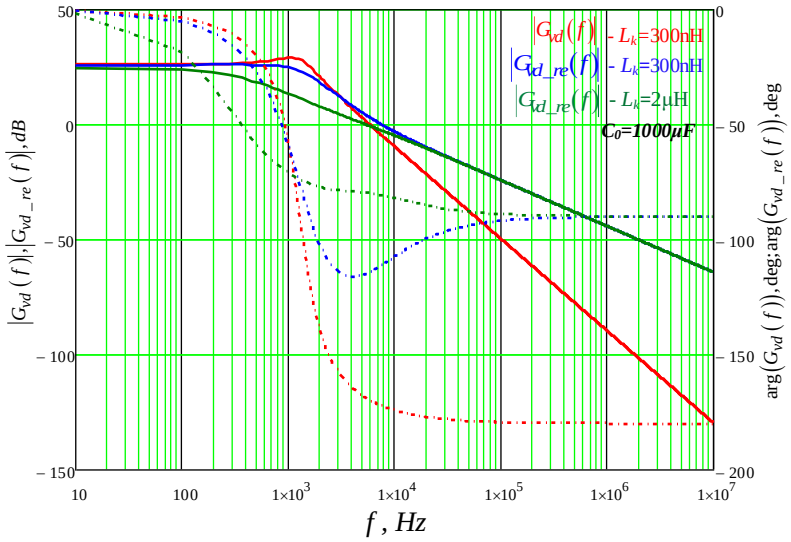

Fig. 4. a. Theoretically obtained Bode diagrams of the magnitude, dB, and phase plots, deg (dashed lines) of PSFB control-to-output transfer functions $G_{vd}(f)$ and $G_{vd\_re}(f)$ for different L_k values at C_0=1000μF

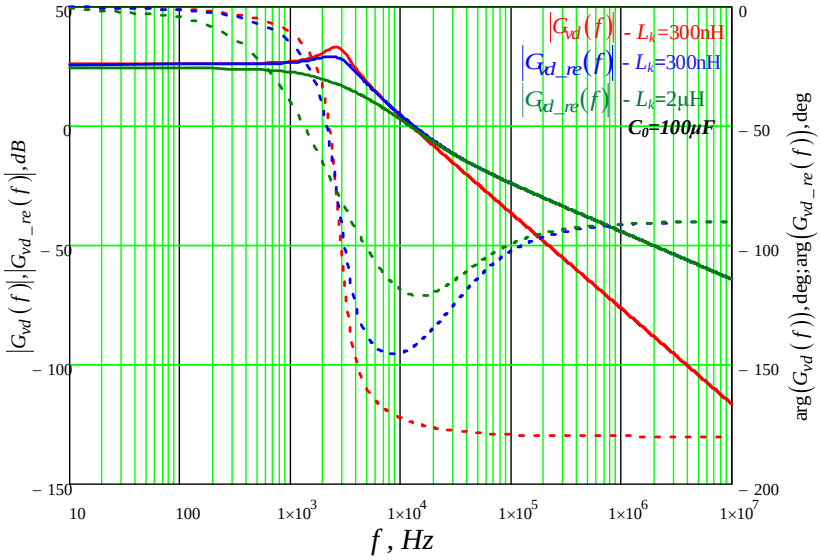

Fig. 4. b. Theoretically obtained Bode diagrams of the magnitude, dB, and phase plots, deg (dashed lines) of PSFB control-to-output transfer functions $G_{vd}(f)$ and $G_{vd\_re}(f)$ for different L_k values at C_0=100μF.

The next step involves studying the influence of loss resistance R_{loss} on the open-loop transfer functions $G_{vd}(f)$ and $G_{vd\_re}(f)$. The results are presented in Fig. 5 for $L_k = 300nH$ and L_k = 2μH, respectively at $R_{loss} = 200m\Omega$ and C_0=1000μF. If we compare the results presented in Fig. 5 and Fig. 4a, we can see that the magnitude indicates that the damping increases as R_{loss} increases, while the crossover frequency remains unchanged. Consequently, when the loss resistance R_{loss} increases, the phase margin around the crossover region is additionally reduced compared to the results presented in Fig. 4a.

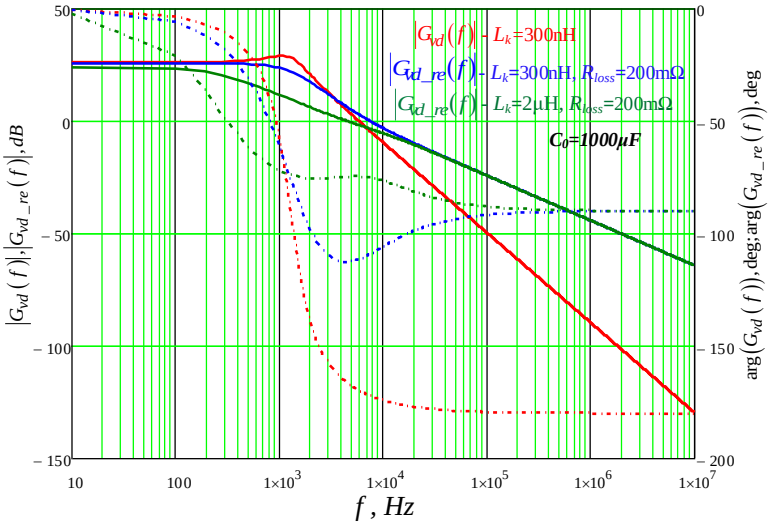

Fig. 5. Magnitude, dB, and phase plots, deg (dashed lines) of PSFB control-to-output transfer functions for different R_{loss} values of L_k =300 nH.

The obtained results demonstrate the necessity of precise calculation in the design of ZVS-PSFB control, particularly with regard to the total losses generated by the commutating inductance (including transformer leakage inductance), switching elements, and passive components.

2.3 Design considerations of a type 2 compensator with an optocoupler

The LTC3722-1 controller enables current control. Thus, a Type 2 compensator circuit needs to be selected. According to [6, 8], the configuration for an isolated current-mode ZVS-PSFB converter is based on the LT1431 programmable reference and an optocoupler MOC207M as shown in Fig. 6.

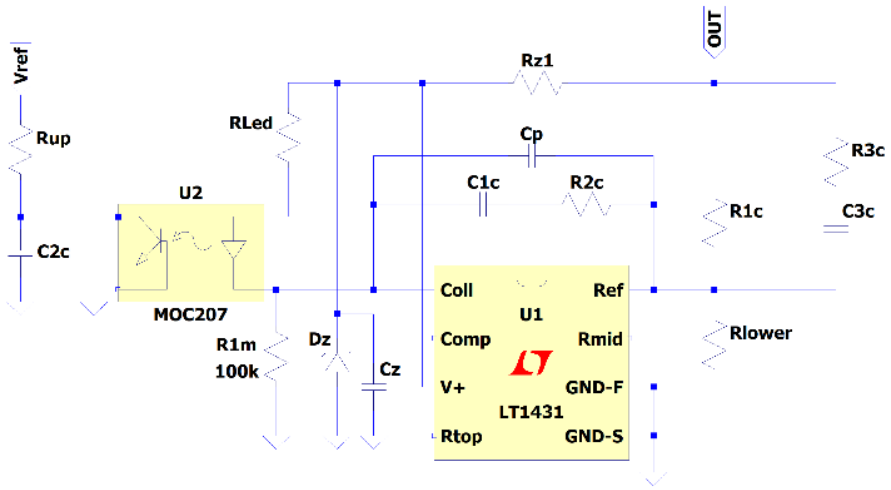

Fig. 6. Configuration of compensator with LT1431 and MOC207M optocoupler

It should be noted that the optocoupler Current Transfer Ratio (*CTR*) is influenced by forward current and temperature, though nominal values are typically assumed in analysis. The parallel collector-emitter parasitic capacitance of the optocoupler is negligible compared to the capacitor C_{2c} and is therefore omitted in calculations.

When R_{Led} is directly connected to the output node, the output ripple is transferred through it, thereby coupling into the modulation path. This interaction gives rise to a zero–pole pair that significantly affects the stability of the control loop. Moreover, R_{Led} determines the mid-frequency gain of the feedback network, rendering its proper selection challenging [11]. To alleviate these limitations, a compensating regulator composed of Rz, Dz, and Cz is introduced. This network stabilizes the zener voltage while effectively decoupling R_{Led} from the modulation channel, thereby enhancing overall system stability. A parallel combination of resistor R_{3c} and capacitor C_{3c} with R1c, it forms the additional pole and zero. This setup effectively functions as a Type 3 compensator, but because the added zero cancels the optocoupler pole, the system behaves like a Type 2 compensator, with one zero, one pole, and a mid-band gain. Resistors R_{1c} and R_{lower} are used to provide the reference voltage of 2.5 V for the LT1431. Thus, the standard value of R_{1c} = 9.53 kΩ and R_{lower} = 2.49 kΩ were chosen. The compensator transfer $G_{co}(s)$ function according to [11, 12] can be calculated as follows:

$$G_{co}(s) = -\frac{R_{2c}R_{up}CTR}{R_{Led}R_{1c}} \cdot \frac{\left(1+\frac{1}{s.R_{2c}C_{1c}}\right)[1+s.C_{3c}(R_{1c}+R_{3c})]}{(1+s.R_{up}C_{2c})(1+s.C_{3c}R_{3c})} \tag{10}$$

Figure 4a shows the Bode plots drawn by Mathcad for a nominal input voltage 48 V and 50 percent load. Crossover frequency is around 10 kHz. Let for initial calculations crossover frequency f_c =10 kHz with $\varphi_{boost} \approx 80^o$ to be chosen. The magnitude of G_{vd_re} is (-3.153dB) in the gain curve at 10 kHz, so the compensation network should provide G_{mid} = 3.153 dB to satisfy the requirement of crossover frequency at nominal input voltage and 50 percent load with a phase margin of 70 to 80 percent, because the crossover frequency varies during its full range of operation [12]. Using the design methodology in [11], R_{Led} = 330 Ω and R_{up} =1470 Ω, standard values are selected. From the data sheets of the used optocoupler, MOC207M, $CTR_{\min}$ =100% was considered. The 5.1V zener diode Dz was used and Rz = 470 Ω.

Using (10), the value of R_{2c} is given by

$$R_{2c} = \frac{G_{mid} R_{1c} R_{Led}}{R_{up} CTR_{min}} \tag{11}$$

To achieve a phase shift of +80° at f_c=10 kHz, the frequencies of the zero and pole are derived as follows.

$$f_p = f_c \left[tan(\varphi_{boost}) + \sqrt{[tan^2(\varphi_{boost}) + 1]} \right] \tag{12}$$

$$f_z = \frac{f_c^2}{f_p} \tag{13}$$

The required capacitance C_{1c} is obtained by selecting a value that establishes a zero at the specified frequency.

$$C_{1c} = \frac{1}{2\pi R_{2c} f_{z1}} \text{ where } f_z = f_{z1} \tag{14}$$

The capacitor C_{2c} is given by

$$C_{2c} = \frac{1}{2\pi R_{up} f_{p1}} \tag{15}$$

where pole f_{p1} should be set at the target frequency. As the zero should be set at the optocoupler pole frequency to cancel its effect, for the zero frequency f_{z2} is valid

$$f_{p1} = f_{z2} = \frac{1}{2\pi C3c(R1c + R3c)} \tag{16}$$

The capacitor C_{3c} is calculated to set the pole as follows

$$C_{3c} = \frac{1}{2\pi R_{3c} f_{p2}} \tag{17}$$

where f_{p2} should be set atf_p.

The standard values of $R_{2c} = 3.09k\Omega$, $R_{3c} = 10k\Omega$, $C_{1c} = 56nF$, $C_{2c} = 1.8nF$, and $C_{3c} = 0.12nF$are selected. Due to the exact values of the selected values of resistors and capacitors, the gain, pole frequencies, and zeroes can be slightly different.

Figure 7 shows the Bode plot of the theoretical compensator, G_{co}, loop gain, and loop phase. Furthermore, based on the obtained results, a simulation was performed with LTspice on the designed compensator. A comparison of the theoretically obtained results and those from the simulation shows a very good coincidence, with the relative error between them not exceeding 1%.

The magnitude of the loop gain G_v as a function of the frequency is calculated as

$$|G_v(f)|, dB = 20\, lg|G_{co}(f)G_{vd}(f)| \tag{18}$$

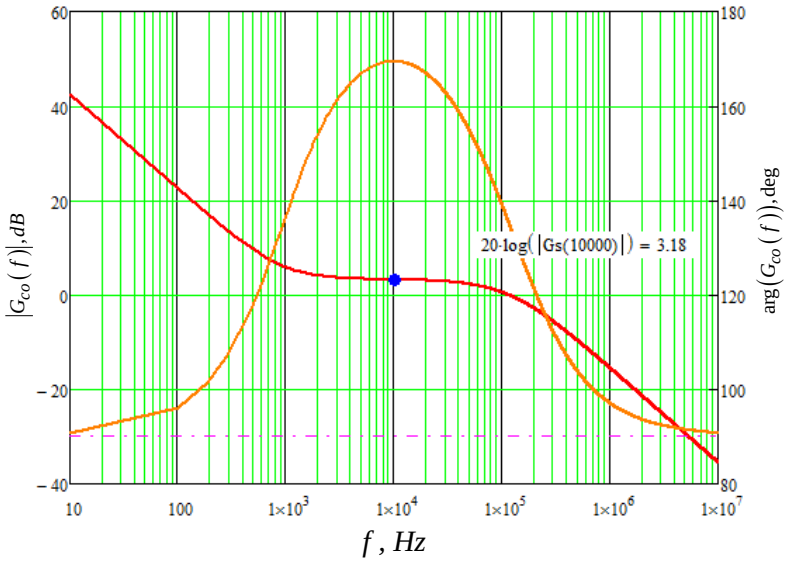

Fig. 7. a. Analytical results of compensator Bode plots $|G_{co}(f)|$– magnitude, dB, and phase, deg

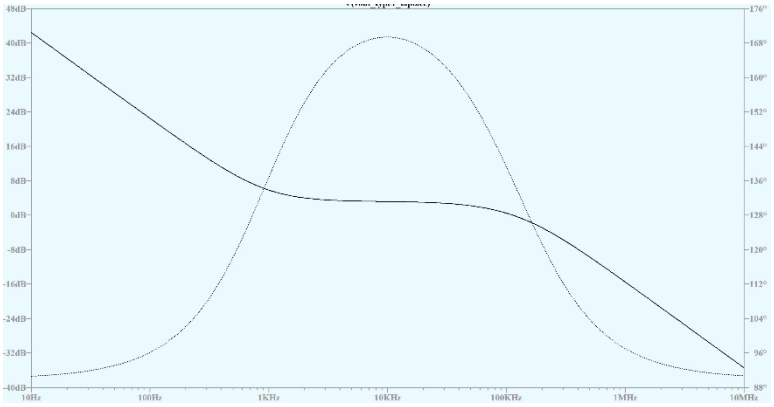

Fig. 7. b. Simulation results of compensator Bode plots $\left|G_{co}\left(f\right)\right|$ – magnitude, dB, and phase, deg

The compensated loop gain plots of the studied ZVS PSFB converter are shown in Fig. 8.

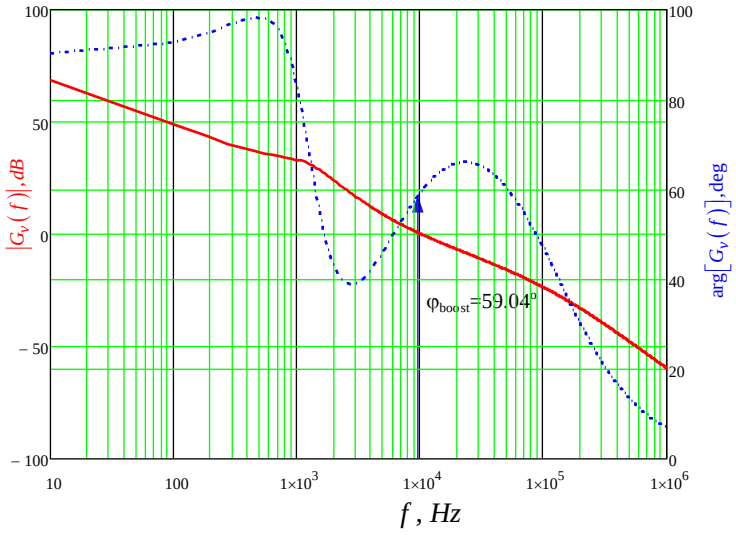

Fig. 8. The compensated loop gain of the studied ZVS PSFB converter – magnitude, dB (red line) and phase plot, deg (blue dashed line)

The theoretical frequency response of the converter plot, unlike the standard Bode plots, is calculated as a distance to zero degrees at the crossover frequency. From the plot, it is seen that the theoretical crossover frequency of the loop is around 10kHz,

and the phase margin at that point is around 59.04° at 50% load and rated input and output voltages.

3. SIMULATION RESULTS

The LTspice simulation circuit is shown in Fig. 9.

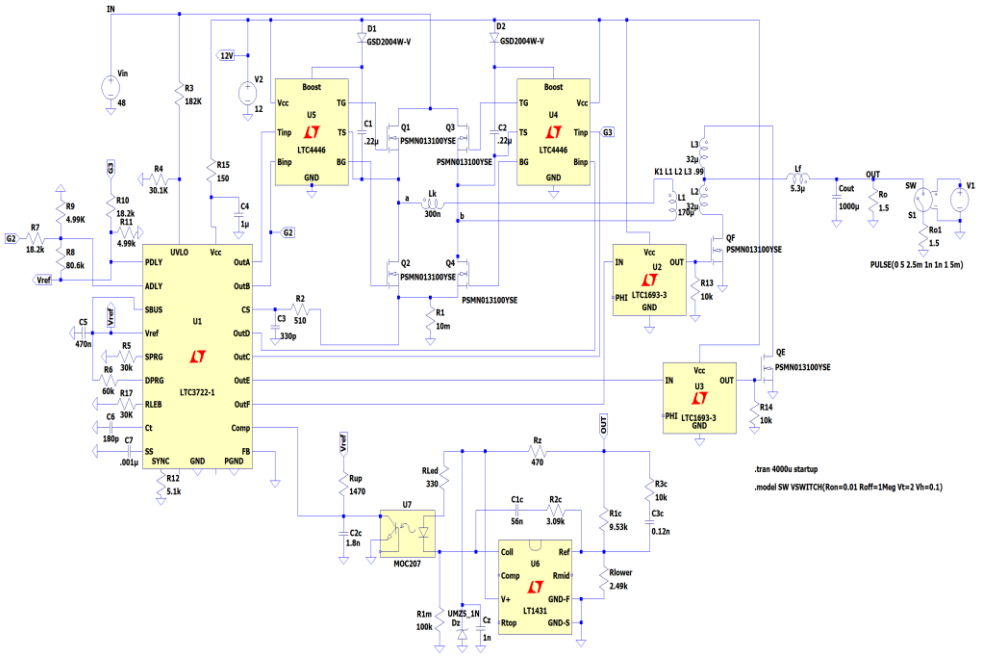

Fig. 9. LTSpice simulation circuit

The circuit is based on the approach given in [8]. The LTC4446 driver is used to control the transistors on both legs of the bridge, while the LTC1693-3 drivers are used to control the synchronous MOSFETs (QE and QF).

With an input voltage of Vin = 48 V, a change in load is simulated from 50% I_0 to 100% I_0 with the elements Sw and the source V1 (PULSE). Figure 10 shows the results, which demonstrate the circuit's response to an abrupt change in load. From top to bottom: 1 plot plane – current trough Lf (I(Lf) green); 2 plot plane – current trough transistor $Q1$ (Id(Q3) red) 3 plot plane – current trough transistors $Q1$ (Id(Q1) blue); 4 plot plane – output voltage (V(out) black). The results demonstrate that the controller processes the impact and achieves the desired output voltage within 0.15ms.

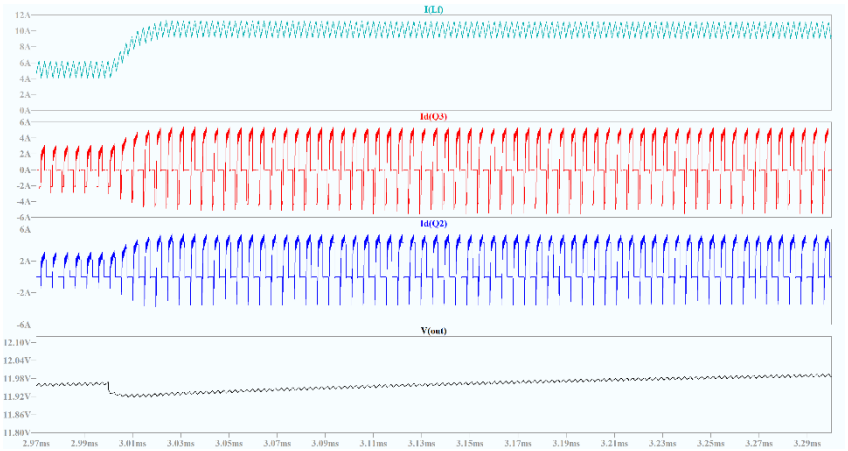

Fig. 10. LTSpice simulation results when load changes – from 50% I_0 to 100% I_0

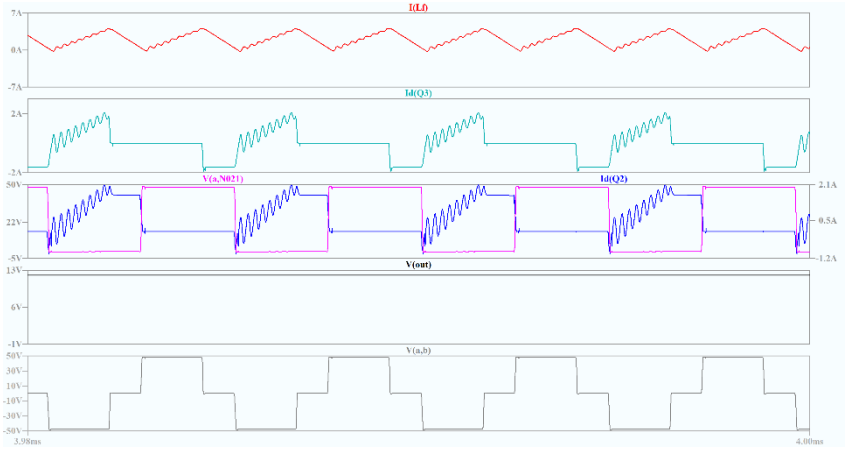

Fig. 11. LTSpice simulation results at I_0<Icrit

Figure 11 shows the results when operating at an output current I_0=2A ($I_0<I_{crit}$) as follows: from top to bottom: 1 plot plane – current trough filter inductance Lf (I(Lf); 2 plot plane – current trough transistor $Q3$ (Id($Q3$) red); 3 plot plane – current trough transistor $Q2$ (Id($Q2$) blue) and $Q2$ drain-source voltage (V(a,N021) pink); 4 plot plane – output voltage Uo (v(out)black); 5 plot plane – voltage u_{ab} (dark grey).

The results confirm that the conditions for ZVS switching of the transistors from the passive leg ($Q1/Q2$), at $I_0<I_{crit}$, are lost.

4. CONCLUSION

This paper analyzes the influence of the added commutating inductance and parasitic elements on the dynamic performance of the zero-voltage (ZVS) phase-shifted full-bridge (PSFB) converter. The open-loop control-to-output transfer functions were discussed. The results indicate that it is necessary to investigate the mutual influence of parasitic elements and losses on the dynamic behavior of the ZVS-PSFB converter. For this purpose, the open-loop control-to-output transfer characteristics both with and without including the equivalent series resistance of the output filter capacitor, R_{ESR}, and the loss of resistance R_{loss} were studied. The obtained results demonstrate the necessity of precise calculation in the design of PSFB control, particularly with regard to the total losses generated by the commutating inductance (including transformer leakage inductance), switching elements, and passive components. The compensator circuit, featuring current-mode control and optocoupler-based feedback, was designed. A simulation study with LTSpice of the converter's operation under the abrupt load changes is presented. The results demonstrate that the controller processes the impact and achieves the desired output voltage within 0.15ms.

As future work, it is necessary to investigate the influence of the added commutating inductance and parasitic elements on the line-to-output transfer function, which represents the sensitivity of output voltage to input voltage variations, as well as the output impedance transfer function. The conducted study has potential applications in both engineering practice and the education of students in power electronics.

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